



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/766,477	01/19/2001	Klan Teng Eng	TI-22944.2	2137
7590	04/21/2006		EXAMINER MITCHELL, JAMES M	
Mark E. Courtney Texas Instruments Incorporated P.O. Box 655474, MS 3999 Dallas, TX 75265			ART UNIT 2813	PAPER NUMBER

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary	Application No.	Applicant(s)	
	09/766,477	ENG ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-25 and 27-38 is/are pending in the application.
- 4a) Of the above claim(s) 29-36 and 38 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 21-25, 27, 28 and 37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to amendment filed June 29, 2005.

Response to Amendment

2. The reply filed on June 29, 2005 is not fully responsive to the prior Office Action because of the following omission(s) or matter(s): does not comply with the requirements of 37 CFR 1.121(c). The correct status of every claim must be indicated thus claims 29-36 and 38 must be labeled as withdrawn. Failure to correct in the next office action will be an intentional non-responsive.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 21, 22, 24, 25 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Cotues et al. U.S. 5,239,447).

5. Cotues (Fig 4, 5) discloses a process of providing a high density module produced by a process comprising the steps of: providing a circuit board (44) having a substantially planar top surface for connection to at least one integrated circuit package (40,); providing an integrated circuit package having a pair of opposing major surfaces

Art Unit: 2813

(Regions near 40, 64) and at least one edge surface (region near 78) disposed between said opposing major surfaces, one of said at least one edge surface having at least one electrical terminal (48) disposed thereon; and electrically connecting (i.e. terminal in contact with items 24, 46) said at least one electrical terminal on said at least one edge surface of said integrated circuit package to said top surface of said printed circuit board at an acute angle with said top surface of said printed circuit board; (cl. 22) a step of electrically connecting at least two said integrated circuit packages to said circuit board at a said edge (i.e. electrical contact formed under edge; Fig 4); (col. 24) solder columns (Fig. 1, item 13) between said integrated circuit and said top of said circuit board; (cl. 25) further including the step of integrally attaching at least three tabs (pads, 4, 24, 54 etc. are projections used to identify/align package and therefore is a tab) package to said circuit board (cl. 27) said package is further defined as being connected at an acute angle between 30 and less than 90 degrees to said circuit board; (cl. 28) wherein said at least one edge surface (i.e. surface crossing to parallel surfaces; shown in Fig 5) is four edge surfaces (Fig 2), each of said four edge surfaces disposed between said major surfaces (parallel surfaces (i.e. regions close to lines indicating 40,84) to form a closed package with said major surfaces.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 27 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cotues et al. (U.S. 5,239,447).

8. Cotues discloses the elements stated in paragraph 6 of this office action and further discloses a high-density module (Fig. 4) where its package is connected to its board less than 90 degrees ("non orthogonal"; Col. 2, Lines 64-65), but does appear to show explicitly that its angle is between 30 and less than 90 degrees. In any event the range, since the general conditions of applicant's invention is disclosed, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure of Cotues 30 or above, since it has been held that where the general working conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

9. Claims 21-25, 27, 28 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U.S. 5,726,492) in combination with Fujisawa et al. (U.S. 6,094,356).

10. Suzuki (Fig 2A, B) discloses a process of providing a high density module produced by a process comprising the steps of: providing a circuit board (32) having a substantially planar top surface for connection to at least one integrated circuit package (25₁); providing an integrated circuit package having a pair of opposing major surfaces (i.e. vertical surfaces) and at least one edge surface (i.e. horizontal portion) disposed

Art Unit: 2813

between said opposing major surfaces, one of said at least one edge surface having at least one electrical terminal (30) disposed thereon; and electrically connecting (i.e. 33) said at least one electrical terminal (30) on said at least one edge surface of said integrated circuit package to said top surface of said printed circuit board; (cl. 22) a step of electrically connecting at least two said integrated circuit packages to said circuit board at a said edge (25₂); (col. 23, 24) with a step of disposing solder columns (33) between said integrated circuit and said top of said circuit board between their terminals (30 & contact under ball on board, 32; not shown); (cl. 25) further including the step of integrally attaching at least three tabs (pads, 30 & contact under ball not shown. are projections used to identify/align package and therefore is a tab) package to said circuit board; (cl. 28) wherein said at least one edge surface (i.e. horizontal portion) is four edge surfaces (i.e. horizontal portion is rectangular; Fig. 11), each of said four edge surfaces disposed between said major surfaces to form a closed package with said major surfaces.

11. Suzuki does not show its package connected to its board at an angle between 30 and less than 90 degrees.

12. Fujisawa (Fig. 3) teaches connecting a package at an acute angle less than 90 degrees.

13. It would have been obvious to one of ordinary skill in the art to connect the package of Suzuki at an angle less than 90 degrees in order reduce the height of the device as taught by Fujisawa (Col. 7, Lines 3-5).

Art Unit: 2813

14. With respect to the angle being between 30 and less than 90 degrees, since the general conditions of applicant's invention is disclosed, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the package of Suzuki between 30 and less than 90 degree, since it has been held that where the general working conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Response to Arguments

15. Applicant's arguments filed June 29, 2005 have been fully considered but they are not persuasive. Applicant contends that Cotues does not show "electrically connecting said at least one electric terminal on said at least one edge surface of said *integrated circuit package* to said top surface of a printed circuit board..." with an emphasis in the *integrated circuit package*, and because there is a dielectric layer on package 40' the package is not electrically connected. Because Cotues explicitly says that the invention applies to a packaged chip (Col. 1, Lines 5-8), all of the electronic devices in the stack (e.g. 41, 40") are therefore integrated circuit with the exception of the top package (40') that acts as a dummy package (14; Fig. 2; Col. 4, Lines 28-31). As for the remaining chip packages, while examiner agrees the terminal (48) is not **electrically connected to a package's edge between two major surfaces**, the claim is not so limited. Because applicant does not affirmatively claim that the terminal along the package edge provides electrical contact for the device immediately above the edge

surface within the opposing major surfaces, Cotues disclosure of a terminal in contact with an edge between opposing surfaces that provides electrical contact for an adjacent package (e.g. through items 48 and 24) it is therefore within the broad scope of applicant's claims.

16. In addition applicant contends that Cotues does not show the steps of electrically and perpendicularly connecting at least two packages to the board. Examiner disagrees. Cotues explicitly shows a stack of packages (Fig. 2, 4) electrically connected (e.g. through items 48 and 24) to a printed circuit board. However, because there is no limitation as claimed (e.g. applicant's claim 22) as argued of "perpendicularly connecting," the argument is deemed moot. As for applicant reference to claim 23 in relation to Cotues, examiner agrees, which is why no rejection based on Cotues was used to reject claim 23. As for applicant's additional argument that Cotues does show alone or in combination of no tabs or that package not being connected at "an acute angle ...," applicant relied on nothing more than mere conjecture (e.g. it's not there), while failing to address examiner's specific rejection regarding those limitation and the prima facie case set forth. Because mere conjecture cannot overcome examiner's prima facie case of obviousness, the rejections are deemed proper. See M.P.E.P 2145 [R-3].

17. Applicant also contends for Suzuki that allegedly because Suzuki shows board/interposer connected to a substrate **rather than the chip** that, "[t]his has nothing whatsoever to do with the claimed invention." [emphasis added]. Examiner is unpersuaded. Because the claim limitation is for an IC package and not just a chip,

than an interposer/substrate for a chip **package**, is within the broad scope of applicant's claims.

18. Lastly, applicant contends that there is no basis for the combination for Suzuki and Fujisawa, because Fujisawa does not show its terminal on an edge. Examiner is unpersuaded, because having terminals on an edge was already known in the art as evidenced by Suzuki, while Fujisawa was only relied on for its teaching of having the package at an acute angle less than 90. Since both references dealt with chip package, and density and the height of packages are a concern in IC fabrication/ packaging, it provides the proper basis why one of ordinary skill in the art would look to Fujisawa. For the reasons stated, *supra*, examiner has found applicant's argument's unpersuasive and the rejection deemed proper.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

Art Unit: 2813


the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm
April 14, 2006


CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800